CAN Newsletter Online

DEBUGGING AND TESTING

For automotive micro-controllers

PLS' debugging and testing solution supports all functions of STMicroelectronics' SPC58 E-line of multi-core automotive micro-controllers. First samples of the MCUs have only recently become available.

(Photo: PLS)

AS A RESULT OF YEARS OF CLOSE PARTNERSHIP with STMicroelectronics, PLS is already able to offer the Universal Debug Engine (UDE) 4.4.6, a debugging and testing solution, for the first samples of STMicroelectronics' SPC58 E-line in ST's multi-core automotive micro-controller (MCU) family.

Features of these automotive MCUs include seven CAN nodes, three power architecture based CPU cores (e200z4d), two of which are capable of lockstep, 6320 KiB on-chip flash memory, 768 KiB SRAM, generic timer module (GTM), hardware security module (HSM), one time-triggered Controller Area Network (TTCAN) node, various analog-to-digital converters, and a range of additional peripheral functions. The target applications for these MCUs include engine management, transmission control, and advanced driver assistance systems (ADAS).

UDE 4.4.6 allows users to program the integrated flash memory as well as the control and management of all active units of the SoC within one consistent user interface. As a result, not only can the main cores be selected as debug target, but also the GTM and HSM or the whole device. This degree of flexibility is supported by a flexible multi-core program loader, which enables loading of program code and data as well as symbol information separately for each individual core.

Management of the individual active units by the debugger is carried out via a special multi-core run control manager, which enables an almost synchronous starting and stopping of the various cores at any time by utilizing logic that is integrated on the chip. In addition, debugging is simplified by the multi-core breakpoints implemented in the UDE. With their help, in shared code a simultaneously acting breakpoint for all cores can be very easily set. Data breakpoints in turn allow the recognition of read and/or write accesses to a variable. Furthermore, even an expected value can optionally be taken into account.

The SPC58 E-line SoCs are also available as emulation devices, which are pin-compatible with the production devices. These emulation devices include additional emulation memory, extensive trigger and filter logic, as well as connections for a serial high-speed interface based on the Aurora protocol. So that developers can abstractly configure the several hundred registers of the additional emulation memory, PLS offers the Universal Emulation Configurator (UEC) with block graphics user interface in addition to the UDE 4.4.6. Measurement tasks can be defined particularly easily with help of the UEC. In doing so, specific states in the target are described by signals. These, in turn, can initiate actions or shift an underlying state machine into a new state.

The UEC helps the user to cope with the limited resources of the on-chip emulation memory. Parallel to this, the implemented Aurora interface offers the possibility to externally record trace data and to carry out a statistical analysis of the program flow such as code coverage and profiling. PLS' Universal Access Device 3+ (UAD3+) with Aurora pod serves for recording, while the evaluation itself is carried out by the UDE.