CAN FD IP Core assists host processor

Fraunhofer IPMS's IP Core supports both ISO CAN FD as well as non-ISO CAN FD. The IP Core also assists the host processor in the management of IP Core communication.

Transponder-ASIC with IPMS_430-Core (Photo: Fraunhofer IPMS)

VISITORS TO THE EMBEDDED WORLD 2016 exhibition held in Nuremberg from February 23 to 25 are invited to stop by booth 583 in hall 4 to get an impression of the CAN FD IP Core. Participants of the accompanying Embedded World conference are also invited to attend the "Migration from CAN to CAN FD – How to Boost Network Performance" presentation to learn more about the steps of the integration of the CAN FD protocols. The presentation is scheduled to begin at 3 pm on Thursday, February 25.

Beyond the CAN FD expansion, the IP Core commands additional functions, which support the host processor in the management of the IP Core communication. Dr. Frank Deicke, Business Unit Manager at Fraunhofer IPMS explains, "The transmit buffer of our IP Core can be operated in first-in-first-out or priority mode. Here, messages of higher priority are automatically sent out first. In addition, our core supports time-triggered CAN (TTCAN) according to ISO 11898-4. With that, it is possible to set timeframes for sending messages at defined time points and mark received messages with a time-stamp. Communications network designers can then therefore ensure that data from individual control units is available in real time«.

The CAN FD IP Core has already been incorporated into ASIC- and FPGA designs and used in the field. It is delivered either as VHDL or Verilog source code and can be implemented into individual control devices or circuits (system-on-chip, FPGA) through its 32-bit controller interface (8 bits and 16 bits, as well as AMBA APB and AHB optional), fully synchronous description and modern clock domain crossing.