Galvanic-isolated CAN FD repeater reference design

Texas Instruments has published an application note describing a two-port repeater using the company's CAN transceivers and an arbitration-logic.

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Block diagram of the isolated CAN FD repeater (Photo: Texas Instruments)

This isolated CAN FD repeater reference design adds electrical isolation between two bus segments. The CAN FD frames on either bus segment side are repeated to the other side. The transceiver and arbitration logic in this reference design support bit rates up to 2 Mbit/s. The design is supplied by a wide range voltage supply between 5 V_{DC} to 33 V_{DC} and protected from high-power transients or lightning strikes by a flat-clamp surge protection device.

Adding bus isolation inside the CAN FD device protects against dangerous electrical transients and eliminates ground loops. When there is no internal isolation, then the device is exposed to some electrical challenges. However, isolation still can be added between non-isolated CAN FD devices by adding an isolated CAN FD repeater into the bus lines. The proposed CAN FD repeater design consists of two TCAN 1042H transceivers. Between these two Texas Instruments has published an application note describing a two-port repeater using the company's CAN transceivers and an arbitration-logic. Galvanic isolated CAN FD repeater reference design transceivers is an isolation barrier and an arbitration logic. The arbitration logic detects which of the two transceivers enter the dominant state first and prevents the loopback of the secondary transceiver side, which would stall the CAN FD network into dominant state otherwise.

Arbitration logic

The arbitration logic is needed to prevent both CAN FD networks to get stuck in dominant state due to the loopback function inside the CAN FD transceivers. The arbitration logic detects, which of the two CAN FD ports is entering the dominant state first. Based on the detection of the first CAN FD side, the arbitration logic blocks the secondary CAN FD side from also asserting dominant state due to the loopback. Once the first CAN FD segment releases the dominant state the arbitration logic starts a time delay unit. After the time delay unit expires, the block of the secondary side is removed. The arbitration logic works in both directions. The delay line unit has an asymmetric delay of the CAN FD line transition. This unit has a delay of 210 ns from dominant state to resistive state and no delay from resistive state to dominant state. The asymmetric delay of 210 ns is needed to support higher bit rates than 2 Mbit/s. Texas Instruments has simulated the arbitration logic. The simulation showed when both sides of the CAN FD interfaces get into a dominant state. Then the side that stays longer in the dominant state wins the bus arbitration, and the port that enters recessive state goes back to receive mode.

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