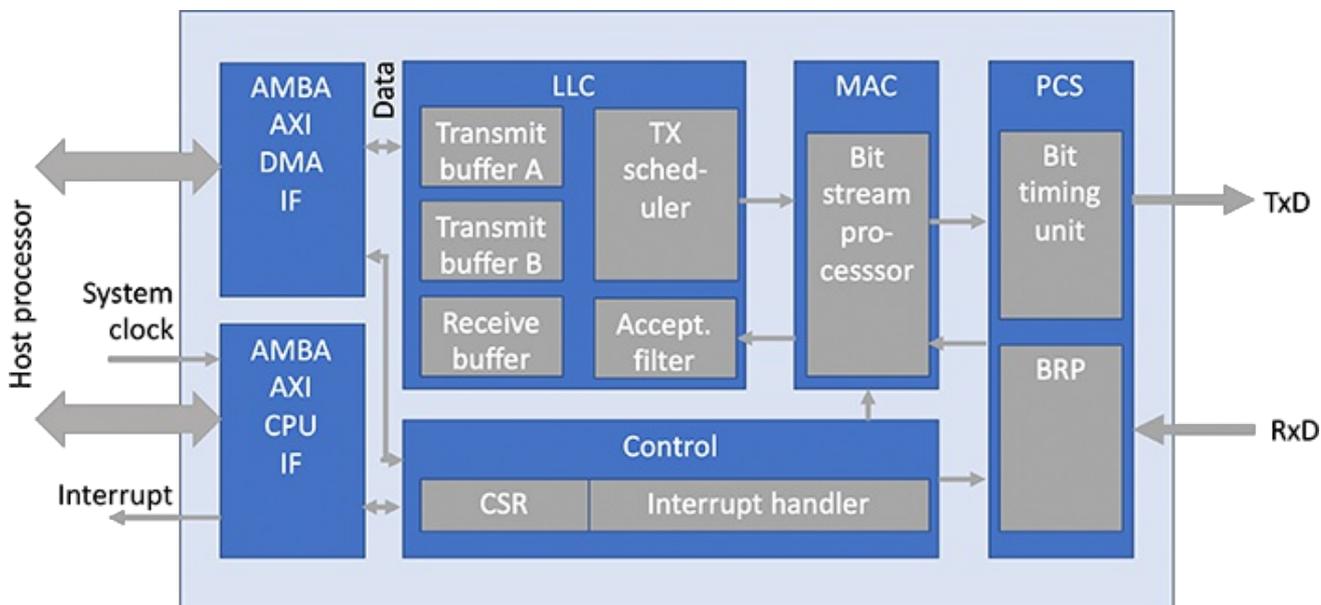


Upgraded to low-power consumption

Arasan has introduced the 2nd generation of its CAN FD core. The re-architected product is now also suitable for FPGA applications.



Block diagram of the CAN FD core suitable for FPGA (field-programmable gate array) implementations (Source: CiA)

Arasan has implemented power saving techniques on its CAN FD core. The 2nd generation CAN controller complies with ISO 11898-1:2015 and supports also TTCAN (time-triggered CAN) level-1 functionality as standardized in ISO 11898-4. Optionally, it can be configured to run the non-ISO CAN FD protocol. “Our 2nd Gen CAN IP is designed to increase reliability, faster error reporting, features advanced Error management unit, prevents data loss during transmission and prevents message collisions,” reported the company.

The CAN IP controller cores can be integrated with the host processor using the AMBA AHB/AXI interfaces specified by ARM. The configurable IP (intellectual property) core supports programmable Interrupts, bit rates, acceptance filters, and flexible buffering schemes. “The IP has been designed in the USA enabling us to support projects requiring US security clearance for support personnel,” stated the company. “The defense and aerospace sectors in addition to automotive are a major target market for Arasan’s fault tolerant CAN IP.”

Additional features include indication of last error type, arbitration lost position, and error thresholds. The implemented listen-only mode enables analysis of CAN/CAN-FD traffic and automatic bit-rate detection. The loopback mode can be used for debug and self-testing during integration and network start.

The deliverables include Verilog RTL source code, a simplified testbench with simulation models to run initial set of tests after release, and a synthesizable netlist. Additionally, the Ip core comes with synthesis scripts and exception lists, a timing report, and a protocol compliance report. Sample firmware and application notes are available, too.

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