Dual HS-CAN transceiver with improved EMC

Company

NXP Semiconductors is one of the market-leading manufacturers of CAN transceiver chips. In the portfolio of the Dutch company, there are transceivers compliant to ISO 11898-2 (CAN high-speed), ISO 11898-3 (CAN fault-tolerant with low-power capability), ISO 11898-5 (CAN high-speed with low-power capability), and CAN single-wire transceivers (SAE J1411). In the pipeline are transceivers compliant to ISO 11898-6 (CAN high-speed with low-power and selective wake-up functionality).

Link

www.nxp.com

Related articles

Minimum distance between CAN nodes (in: CAN Newsletter December 2011, page 12)
CANopen micro-controller with on-chip transceiver (in: CAN Newsletter March 2011, page 28)
CAN transceiver isolating signals and power (in: CAN Newsletter March 2011, page 24)
Combined transceiver for CAN and LIN (in: CAN Newsletter September 2010, page 40)
CAN physical layer protection hints (in: CAN Newsletter March 2010, page 34)

The TJA1048 is a dual high-speed CAN transceiver that provides an interface between a CAN protocol controller and the physical network wires. The chip is suitable for bit-rates up to 1 Mbit/s. It belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1040. It offers improved electro-magnetic compatibility (EMC) and electro-static discharge (ESD) performance.

The chip supports two operating modes individually per transceiver: normal and stand-by. The operating mode can be selected independently for each transceiver via two pins (STBN1 and STBN2).

In normal mode, the transceivers can transmit and receive data via the CANH1/CANL1 and CANH2/CANL2 bus lines. The differential receiver converts the analog data on the bus lines into digital data, which is output on the RXD1/RXD2 pins. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible EME.

In stand-by mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and normal-mode receiver blocks are switched-off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity.

In stand-by mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When the RXD1/RXD2 pins goes LOW to signal a wake-up request, a transition to normal mode will not be triggered until the STBN1/STBN2 pins are forced HIGH. A dedicated wake-up sequence (specified in ISO 11898-5) must be received to wake-up the transceiver from a low-power mode. This filtering is necessary to avoid spurious wake-up events due to a dominant clamped CAN network or dominant phases caused by noise or spikes on the bus.

A valid wake-up pattern consists of: A dominant phase of at least $t_{wake(busdom)}$ followed by a recessive phase of at least $t_{wake(busrec)}$ followed by a dominant phase of at least $t_{wake(busdom)}$. The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern. The RXD1/RXD2 pins will remain recessive until the wake-up event has been triggered.

After a wake-up sequence has been detected, the transceiver will remain in stand-by mode with the bus signals reflected on the RXD1/RXD2 pins. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on the RXD1/RXD2 pins in stand-by mode.

A wake-up event will not be registered if any of the following events occurs ▷

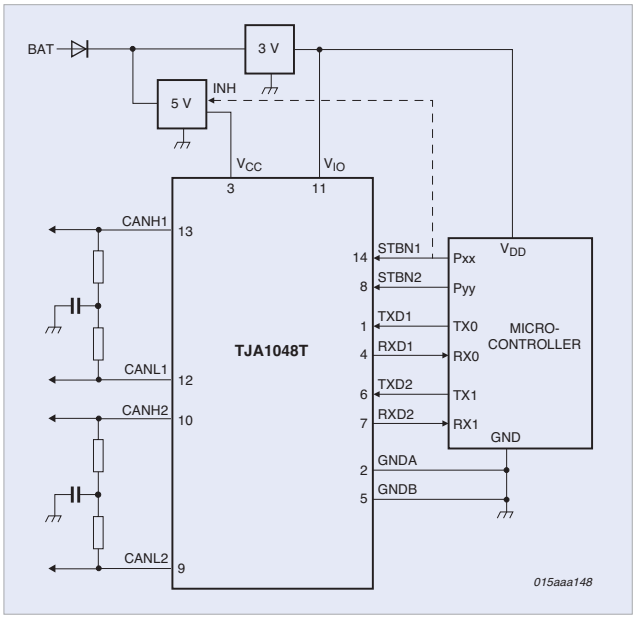
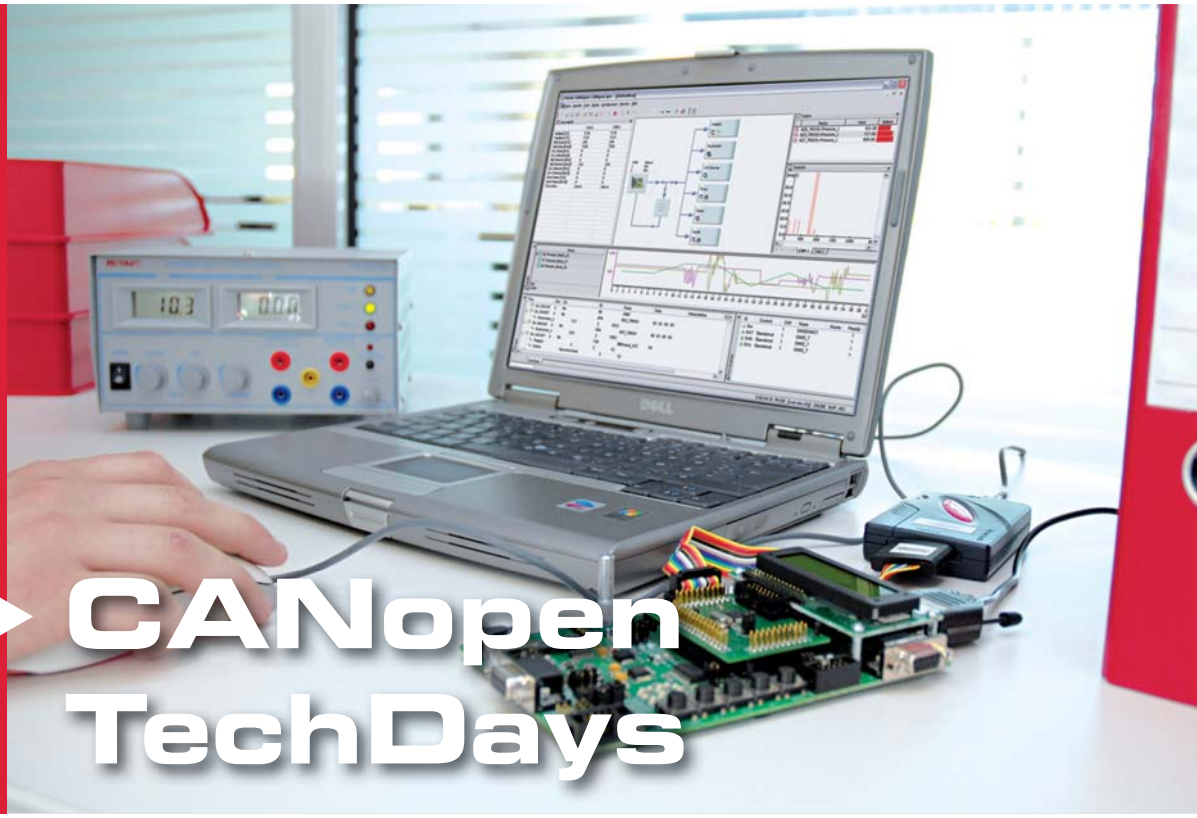


Figure 1: Typical application with 3-V micro-controllers



Beschleunigen Sie Ihre CANopen-Entwicklung

Erfahren Sie auf den kostenlosen Vector CANopen TechDays, wie Sie Ihre CANopen-Komponenten und -Systeme noch effizienter entwickeln. Anhand von Grundlagenvorträgen, praktischen Anwendungstipps und Tool-Demonstrationen zeigen die CANopen-Spezialisten von Vector wie sich durch den Werkzeugeinsatz Wettbewerbsvorteile ergeben können. Der Weg zur richtigen Teststrategie und CANopen-Konformität wird anhand von Live-Demonstrationen anschaulich vermittelt.

Die Veranstaltungen finden statt am:

- **25. September in Düsseldorf**
- **26. September in Berlin**
- **09. Oktober in München**
- **11. Oktober in Stuttgart**

Beginn 9:00 Uhr, Ende gegen 14:00 Uhr, selbst mitgebrachte CANopen-Hardware können Sie auf CANopen-Konformität prüfen lassen.

Weitere Informationen und Anmeldung:
www.vector.com/canopen_techday

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Vector CANopen TechDays 2012

25.09.2012 in Düsseldorf
26.09.2012 in Berlin
09.10.2012 in Aschheim-Dornach (bei München)
11.10.2012 in Stuttgart

09:00 **Begrüßung**

09:15 **Wettbewerbsvorteile durch Werkzeugeinsatz bei CANopen**

> Einführung in die Basiseigenschaften von CANopen
> Wo helfen Softwarewerkzeuge in diesem Umfeld?
> Einfluss der Basiseigenschaften auf die Testbarkeit
> Was kann man vom CANopen Conformance Test erwarten – und was nicht?
> Was muss vom Anwender darüber hinaus getestet werden?
- Weitgehende Protokollkonformität
- Timing
- Applikatives Verhalten

10:00 **Kaffeepause**

10:30 **Live Demonstration 1: Werkzeugeinsatz im CANopen-Entwicklungsumfeld**

> Wie bekomme ich die EDS-Datei für mein CANopen-Gerät?
- Aktuelle Marktsituation, Probleme und Lösungsvorschläge
- Einführung in den EDS-Editor CANeds

> Erste „CANopen Gehversuche“
- Einführung in die CANopen-Toolumgebung
- Tracing, Logging, Stimulation: Was ist notwendig und sinnvoll?
- Woher bekomme ich eine CANopen-Datenbasis?

11:15 **Live Demonstration 2: Teststrategien für CANopen**

> Unterscheidung Gerätetest/Applikationstest
> Wie prüfe ich die CANopen-Konformität?
- CiA Conformance Test vs. CANoe.CANopen
- Wie baue ich eine Testumgebung auf?
- Automatische Testerstellung in wenigen Minuten

> Wie erstelle ich einen Applikationstest?
- Erstellung eines Testszenarios basierend auf einer generierten Testumgebung

12:00 **Kaffeepause**

12:15 **Flexibles Testen mit dem VT System**

> Einführung in das Vector VT System (I/O-Schnittstellenmodule für den Gerätetest)
> Einfacher Aufbau einer Testumgebung
> Komfortables Erstellen von Testsequenzen mit dem Test Automation Editor

13:00 **Diskussion und Fragen**

13:15 **Mittagessen**

14:00 **CANopen-Konformitätsprüfung mit realer Hardware** (optional, je nach Bedarf)
Danach offenes Veranstaltungsende. Bei einem Kaffee beantworten unsere Experten noch Ihre individuellen Fragen oder testen Ihr mitgebrachtes CANopen-Gerät.

Weitere Informationen und Anmeldung:
www.vector.com/canopen_techday

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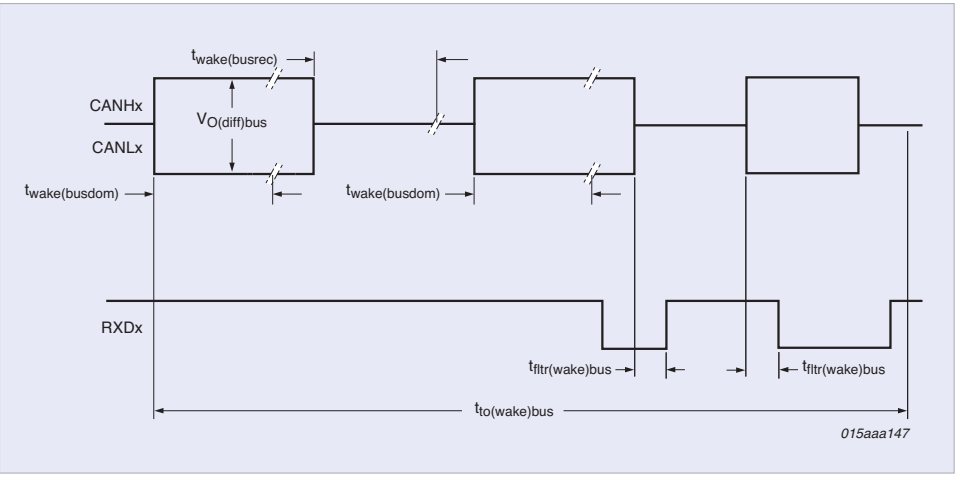

Figure 2: Wake-up time diagram

while a wake-up sequence is being transmitted:

- The transceiver switches to normal mode

The complete wake-up pattern was not received within $t_{to(wake)bus}$

- A V_{IO} under-voltage is detected

If any of these events occurs while a wake-up sequence is being received, the internal wake-up logic will be reset and the complete wake-up sequence will have to be re-transmitted to trigger a wake-up event.

Fail-safe features

A 'TXD dominant time-out' timer is started when the TXD1/TXD2 pins are set LOW. If the LOW state on these pins persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset, when the TXD1/TXD2 pins are set HIGH. The TXD dominant time-out time also defines the minimum possible bit-rate of 40 kbit/s. The chip has two TXD dominant time-out timers that operate independently of each other.

The internal biasing is achieved by means of pull-up and pull-down resistors. The TXD1 and TXD2 pins have internal pull-ups to V_{IO}. The STBN1 and STBN2 pins have internal pull-downs to GND_A and GND_B. This ensures a safe, defined state if any of these pins is left floating. The GND_A and GND_B pins must be connected together in the application. The pull-up/pull-down currents flow in these pins in all states. The TXD1 and TXD2 pins should be held HIGH in stand-by mode to minimize stand-by currents; the STBN1 and STBN2 pins should be held LOW.

Should the supply voltage drop below the V_{CC} under-voltage detection level, both transceivers will switch to stand-by mode. The logic state of STBN1 and STBN2 pins will be ignored until V_{CC} has recovered. Should V_{IO} drop below the V_{IO} under-voltage detection level, the transceivers will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, both output drivers will be disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers will recover independently once TXD1/TXD2 has been reset to HIGH. Including the TXD1/TXD2 condition prevents output driver oscillation due to small variations in temperature.

The V_{IO} pin should be connected to the micro-controller supply voltage. This will adjust the signal levels of the TXD1, TXD2, RXD1, RXD2, STBN1 and STBN2 pins to the I/O levels of the micro-controller. The V_{IO} pin also provides the internal supply voltage for the transceiver's low-power differential receiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on the V_{CC}. ◀

TJA1048 features

- *Two transceivers based on TJA1042 combined monolithically in a single package*
- *ISO 11898-2 and ISO 11898-5 compliant*
- *Suitable for 12-V and 24-V systems*
- *Low electro-magnetic emission (EME) and high electromagnetic immunity (EMI)*
- *V_{IO} input allows direct interfacing with 3-V to 5-V micro-controllers*
- *Available in SO14 and HVSON14 packages)*
- *Low-current stand-by mode with host and bus wake-up capability*
- *Transceiver disengages from the bus when not powered up (zero load)*
- *Wake-up receiver powered by V_{IO}; allows shut down of V_{cc}*
- *Bus pins protected against transients in automotive environments*
- *Transmit data (TXD) dominant time-out function*
- *Under-voltage detection on pins V_{cc} and V_{IO}*
- *Thermally protected*

Reference

TJA1048 product data sheet: Dual high-speed CAN transceiver with stand-by mode.